ANALYSIS AND DESIGN OF LOW POWER PULSE TRIGGERED FLIP-FLOP

Mrs.A.Kamatchi Devi[1], Mrs.S.Priyanka[2], Mr.S.Vignesh[3]

Assistant professor[3]

[1,2,3]*Department of Electronics and Communication,*

Theni Kammavar Sangam College of Technology, (India)

ABSTRACT

Power consumption is one of the major design issues in the Very Large Scale Industry design. In this work, various design techniques for a low power clocking system are analyzed. A low-power flip-flop (FF) design featuring a latch based on a signal feed-through scheme and an explicit type double edge triggered pulse generator is presented. The proposed design aims to overcome the long discharging path problem that exists in conventional explicit type pulse-triggered FF (P-FF) designs and also achieves better speed and power performance. When designing a digital system deciding on the clocking strategy is one of the most important decisions. To further reduce power on the clock tree and the clocked transistors in pulse generator double-edge clocked pulse generator is utilized. By using these techniques balanced and improved performance among power, delay, and area, design space exploration is achieved.

Keywords: Double Edge Triggering, Flip-Flop (FF), Low Power, Pulse Triggered, Signal Feed-Through.

I. INTRODUCTION

The primary concerns of the VLSI circuit design were area, power and speed. The enhancement of chip scale of design made excessive amount of heat and power dissipation. This also degrades the system performance and lifetime. In addition, power dissipation has the direct impact on packaging cost of the chip and coding cost of the system. This also made power consumption as the major concern. In a VLSI system the clock system, which consists of clock distribution network and sequential elements is one among the more power consuming components. By reducing power consumption of the flip-flop we can reduce total power consumption of the system.

Flip-flop is the basic storage element widely used in all kinds of digital circuits. In the previous designs Master-slave flip-flops are often used. This can be replaced by a pulse triggered flip-flop which requires a single latch and thereby reducing the chip area and overall power consumption. This also reduces the complexity of the circuit. Pulse triggered flip-flops are classified as implicit pulse triggered and explicit pulse triggered flip-flop. In an Implicit pulse triggered flip-flop pulse generator is built in logic of the latch structure. But it exhibit longer discharging path problem. In an explicit pulse triggered flip-flop pulse generation and latch structure design are separate. Due to the separate pulse generator explicit type consumes more power. But this can be tolerable while large numbers of latch structure sharing the same pulse generator circuit. Implicit

pulse triggered design such as conditional pulse enhancement based P- flip-flop, modified hybrid latch flip-flop and the explicit pulse triggered flip-flops namely ep-DCO (explicit pulse triggered flip-flop Data close to output), conditional discharge flip-flop and static conditional discharge flip-flops are also reviewed here.

II. EXISTING DESIGN

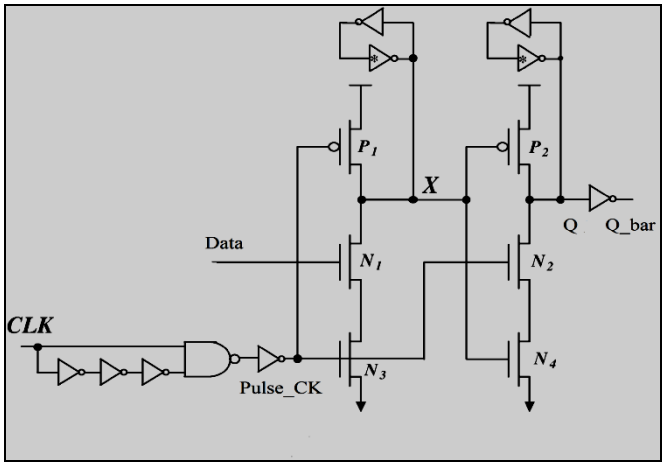

Fig.1. Explicit pulse triggered Data close to Output

Fig.1shows the schematic diagram of the Explicit pulse triggered data close to output. It contains a NAND logic based pulse generator and a true single phase clock structured latch. This design has a major drawback i.e., the internal node X discharges on every rising edge of the clock in spite of presence of static input 1.This causes large switching power dissipation. This problem can be overcome by the techniques such as conditional capture, conditional discharge and conditional precharge.

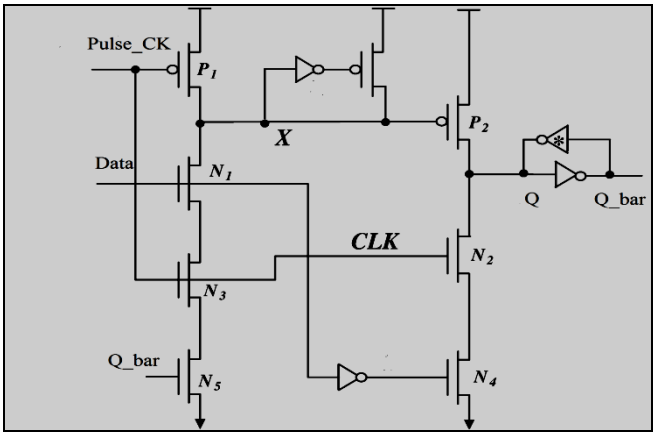

Fig.2. Conditional discharge Flip-flop

Conditional Discharge Flip-flop design is shown in Fig. 2.In this design control is employed in the discharging path. Discharging path will be switched off by inserting an NMOS transistor controlled by the output signal in the discharging path as long as input is stable at high i.e., when the input data undergoes a low to high transition the output Q changes to high and Qbar to low. This will disable the discharge path as long as the input data remains high.

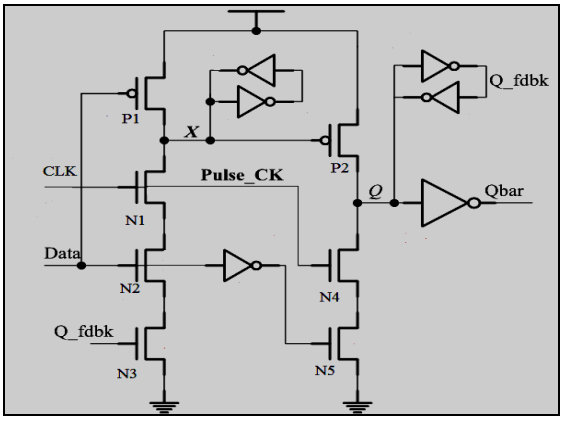

Fig.3. Static Conditional Discharged Flip - flop

Fig.3. shows the Static conditional discharge Flip-flop design. This structure differs from the CDFF design by using the static latch structure. So, the node X is not needed to be precharged periodically. This design exhibits longer D-to-Q delay than CDFF technique. Both the techniques face a worst case delay. This can be overcome by powerful pull down circuitry which consumes more power.

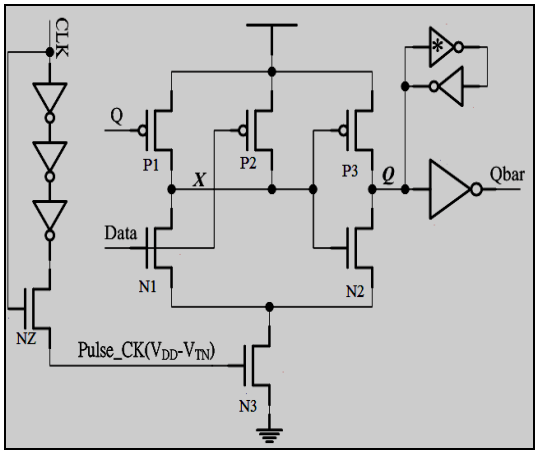

Fig.4. Modified Hybrid Latch Flip - flop

The schematic diagram of Modified Hybrid Latch Flip-flop is shown in Fig.4. This design is based on the static latch structure, which avoids the periodical precharging of the node X. Here weak pullup transistor P1 controlled by the signal Q used to maintain the node level at high when Q is zero. This eliminates the unnecessary discharging problem at the node. Since the node is not predischarged longer D-to-Q delay occurs during 0 to 1 transition. In certain cases node X becomes floating.

The proposed explicit pulse triggered flip-flop design based on signal feed through scheme provides an improved power and delay performance. This will be discussed in the III section. Result and conclusion will be discussed in the IV and V section.

III. PROPOSED DOUBLE EDGE PULSE TRIGGERED FLIP FLOP DESIGN

The four circuits considered above experience the worst case timing during the data transitions occurring at 0 to 1. The proposed design employs a signal feed-through technique to improve this delay. The SCDFF design and the proposed design have the static latch structure and a conditional discharge scheme to avoid continuous switching at an internal node. The major differences made in this design lead to a unique TSPC latch structure

and make the proposed design distinct from the previous one. An approach suitable for high-performance, low-power applications is the use of dual-edge-triggered (DET). Substantial power savings in the clock distribution network can be achieved by reducing the clock frequency by one half. This can be done if every clock transition is used as a time reference point instead of using only one transition of the clock (leading edge or trailing edge).

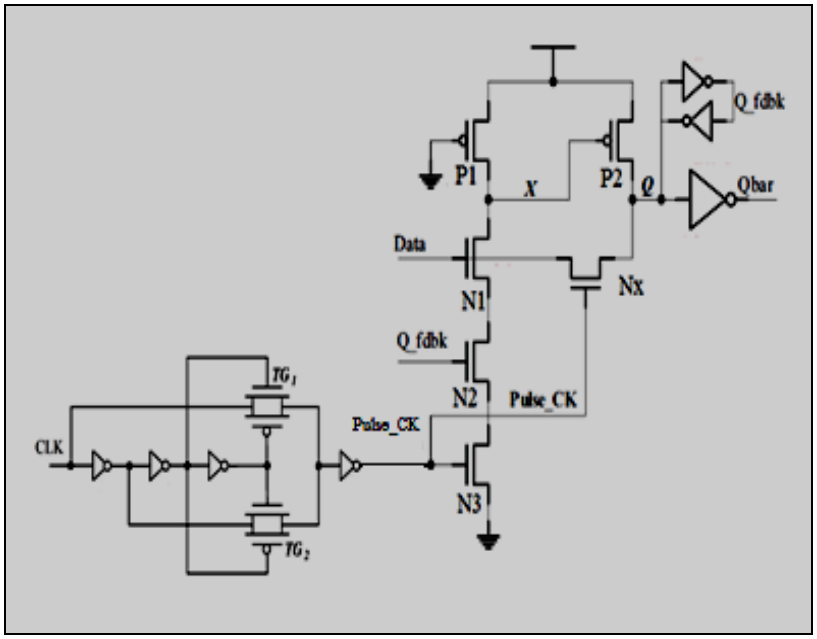

Fig.5. Schematic of Proposed Double Edge Pulse Triggered Flip-flop

In the proposed design pulse generator circuit is designed using the transmission gates. This pulse generator is suitable for double-edge sampling. In the first stage of the TSPC latch a pull-up pMOS transistor with gate connected to the ground is used which gives rise to a pseudo-nMOS logic style design. Thus the charge keeper circuit for the internal node X can be saved. This approach also reduces the load capacitance of node X, which makes the circuit simpler. Also a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Then the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed-through. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the proposed design shows the most balanced delay behaviors.

The main advantage of this approach is that the system operates at half the frequency of a conventional single edge clocking design style while obtaining the same data throughput. Consequently, the power consumed by the

clock generation and distribution system is roughly halved for the same clock load. In addition, less aggressive clock subsystems can be built which further reduce power consumption and clock uncertainties. Dual-edge clocking is based on dual-edge-triggered storage elements (DETSE) capable of capturing data on both the rising and falling edge of the clock. The use of a dual-edge clocking strategy requires precise control of the arrival of both clock edges. This can be satisfied with reasonably low hardware overhead. In addition, the clock uncertainty resulting from the variation of the duty cycle can be partially absorbed by the storage element. Dual edge clocked P-FF design comprised of latch and flip-flop. This design is capable of transferring the data at both the edge of the clock; i.e., at the positive edge of the clock as well as the negative edge of the clock. This can be accomplished by the usage of two transmission gate at the pulse generation of clock.

This design is efficient compared to the double edge triggered method. Also this design occupies only smaller area compare to the other designs. Thus this design is produce a balanced power, delay and area values. The clock load of this flip-flop is comparable to that of a single-edge-triggered flip-flop. This makes a DECPFF a viable option for both high performance and low-power systems.

IV. RESULTS

By using the H-SPICE simulations in 90nm technology at room temperature the results such as Power, Delay and Power Delay Product (PDP) were obtained. The operating condition used in simulations is 500MHz/1.8 V. The output of the FF is loaded with a 1-F capacitor.

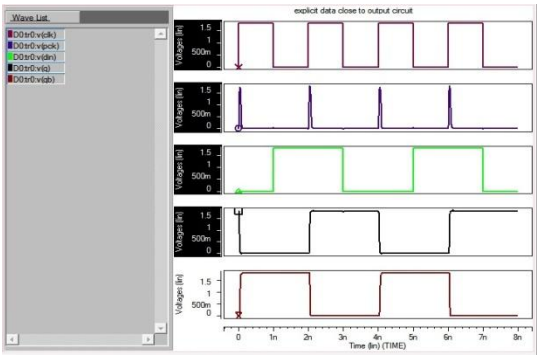

Fig.6. Waveform of Explicit Pulse Triggered Data close to Output

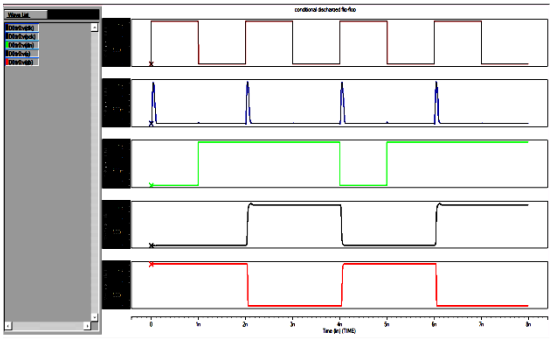

Fig.7. Waveform of Conditional Discharge Flip-flop

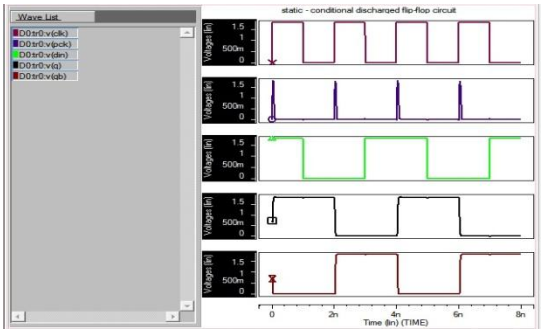

Fig.8. Waveform of Static Conditional Discharge Flip-flop

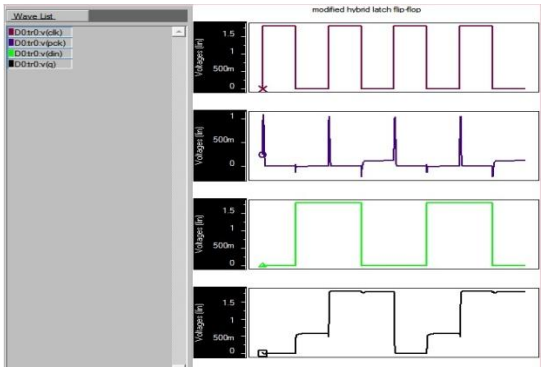

Fig.9. Waveform of Modified Hybrid Latch Flip-flop

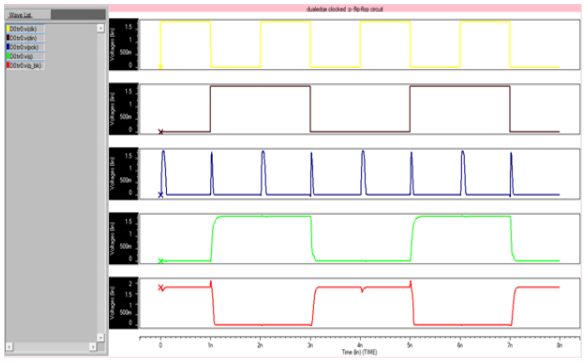

Fig.10. Waveform of Proposed Double Edge Pulse Triggered Flip-flop

Table.1 Result Comparison of various Flip-flop Designs

Flip-flop Designs	**Power(uw)**	**Delay(ns)**	**PDP(fJ)**
Explicit Pulse Triggered Data close to Output	74.921	4.0492	303.37
Static Conditional Discharge Flip-flop	70.495	2.0493	144.68
Conditional Discharge Flip-flop	61.464	4.0376	248.17

Modified Hybrid Latch Flip-flop	192.48	2.0078	386.45
Proposed dual edge Pulse Triggered Flip-flop	45.170	3.0335	137.02

V. CONCLUSION

In this paper, a novel low-power and high speed pulse triggered flip-flop and the double edge triggered design of the same has been proposed to reduce the power consumption. Thus several design techniques are designed to identify the reduction in power consumption. By providing the signal feed-through from input source to the internal node of the latch, in the proposed design to shorten the transition time and enhance both power and speed performance. This design is also implemented by using the double edge clocked technique. Substantial power savings in the clock distribution network can be achieved by reducing the clock frequency by one half. Hence it is concluded that this design achieves low power consumption. Shift registers has been constructed to show how the power will decrease as the sharing of a single pulse generator among multiple flip- flops is increased can be extended for the future work.

REFERENCES

[1] H. Kawaguchi and T. Sakurai, A reduced clock-swing flip-flop (RCSFF) for 63% power reduction, IEEE J. Solid-State Circuits, vol. 33, no. 5, pp. 807–811, May 1998.

[2] K. Chen, A 77% energy saving 22-transistor single phase clocking D-flip-flop with adoptive-coupling configuration in 40 nm CMOS, in Proc. IEEE Int. Solid-State Circuits Conf., Nov. 2011, pp. 338–339.

[3] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, Conditional pushpull pulsed latch with 726 fJops energy delay product in 65 nm CMOS, in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2012, pp. 482–483.

[4] H. Partovi, R. Burd, U. Salim, F.Weber, L. DiGregorio, and D. Draper, Flow-through latch and edge-triggered flip-flop hybrid elements, in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 1996,pp. 138–139.

[5] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, A new family of semi-dynamic and dynamic flip-flops with embedded logic for high-performance processors, IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 712–716, May 1999.

[6] V. Stojanovic and V. Oklobdzija, Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems, IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[7] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors, in Proc. ISPLED, 2001, pp. 207–212.

[8] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J. Sullivan, and T. Grutkowski, The implementation of the Itanium 2 microprocessor, IEEE J. Solid-State Circuits, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.

[9] S. Sadrossadat, H. Mostafa, and M. Anis, Statistical design framework of sub-micron flip-flop circuits considering die-to-die and within-die variations, IEEE Trans. Semicond. Manuf., vol. 24, no. 2, pp. 69–79, Feb. 2011.

[10] M. Alioto, E. Consoli, and G. Palumbo, General strategies to design nanometer flip-flops in the energy-delay space, IEEE Trans. Circuits Syst., vol. 57, no. 7, pp. 1583–1596, Jul. 2010.

[11] M. Alioto, E. Consoli, and G. Palumbo, Flip-flop energy/performance versus Clock Slope and impact on the clock network design, IEEE Trans. Circuits Syst., vol. 57, no. 6, pp. 1273–1286, Jun. 2010.

[12] M. Alioto, E. Consoli, and G. Palumbo, Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part I methodology and design strategies, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 5, pp. 725–736, May 2011.

[13] M. Alioto, E. Consoli and G. Palumbo, Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part II - results and figures of merit, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 5, pp. 737–750, May 2011.

[14] B. Kong, S. Kim, and Y. Jun, Conditional-capture flip-flop for statistical power reduction, IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[15] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, Conditional precharge techniques for power-efficient dual-edge clocking, in Proc. Int. Symp. Low-Power Electron. Design, Aug. 2002, pp. 56–59.

[16] P. Zhao, T. Darwish, and M. Bayoumi, High-performance and low power conditional discharge flip-flop, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May 2004.

[17] M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, A low-power static dual edgetriggered flip-flop using an output-controlled discharge configuration, in Proc. IEEE Int. Symp. Circuits Syst., May 2005, pp. 2429–2432.